LHCb PreShower Photodetector and Electronics

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OUTLINE

✓ INTRODUCTION
✓ PHOTODETECTOR PERFORMANCE
✓ THE AGING PROBLEM
✓ THE NEW DESIGN OF THE ELECTRONICS
✓ CONCLUSIONS
INTRODUCTION

MAIN PURPOSES OF THE LHCb PRESHOWER:

✓ LEVEL 0 TRIGGER: ELECTRON/HADRON ID
✓ ELECTRON/PHOTON ENERGY MEASUREMENT

Please refer to the talks of:

➢ Evgueni Gushin, for a description of the PreShower of the LHCb experiment (detector session),

➢ Frédéric Machefert, for the overview of the LHCb calorimetry electronics (this session).
INTRODUCTION

- PreShower scintillation light is extracted with helicoidal Wavelength Shifting Fibres.
- Both WLS fibres ends are connected to long clear fibres.
- Blocks of 64 cells are coupled to 64-anodes PMT.

The Photodetector: 8 STAGES Multianode PhotoMultipliers from the Hamamatsu Company

A dedicated test bench has been developed for MultiAnode PMT qualification
PHOTODETECTOR PERFORMANCE

1) PHYSICS CONSTRAINTS

2) THE TEST BENCH

3) NON-UNIFORMITIES

4) LINEARITY

5) MAGNETIC FIELD BEHAVIOUR
1) PHYSICS CONSTRAINTS

Two Main functionalities:

**detect low energy deposits for trigger:** Minimum Ionising Particles energy deposit (MIP) corresponding to 20-30 photoelectrons.

**measure large energy deposits:** Up to 100 Minimum Ionising Particles energy deposit.

10 bits dynamics required with 1 MIP = 10 ADC counts

Good Linearity all along the dynamics

Low cross-talk
2) THE TEST BENCH

allows fine structure tests of

- PMT Uniformity, linearity and cross-talk
- Makes use of both VFE + FE prototypes Read Out
2) THE TEST BENCH (in details) : LIGHT SYSTEM

- Studied MultiAnodes PMT
- MonoAnode PMT as reference

- OPTICAL QUARTZ FIBRE
- OPTICAL COUPLER
- BALL LENS
- LED
- µ-LENS
- FILTER

- 3 mm
- 2.5 cm

- MIMICS A PARTICLE SIGNAL
- THE DYNAMICS OF THE FILTRE IS >10³
- CONTROLL LIGHT WITH A REFERENCE PMT (ATLAS TILECAL)
2) THE TEST BENCH (in details): PMT TRANSLATION TABLE

- ALLOWS \((x,y)\) TRANSLATIONS
- THE FIBRE: 200 \(\mu m\) active core
- PMT DISPLACEMENTS: 100\(\mu m\)
- ACCURATE TESTS OF PIXELS STRUCTURE
PHOTODETECTOR PERFORMANCE

2) THE TEST BENCH (in details): ELECTRONICS, READ-OUT

- VFE BOARD PROTOTYPE
- FE BOARD PROTOTYPE
- VME ACQUISITION
- ALL COMMANDS IN LABVIEW
3) NON-UNIFORMITIES

5 Ma-PMT have been extensively studied. The non-uniformities of the anodes were never measured larger than a ratio (1:3).
4) NON-LINEARITY

GOOD LINEARITY ALL OVER THE DYNAMICS RANGE

LINES ARE +/-5%
PHOTODETECTOR PERFORMANCE

4) BEHAVIOUR IN MAGNETIC FIELD

FEW TENS OF GAUSS AT THE Ma-PMT LOCATION
4) BEHAVIOUR IN MAGNETIC FIELD

IMPORTANT LOSS OF GAIN WAS MEASURED; A SHIELDING HAS BEEN DESIGNED. IT HAS BEEN CHECKED THAT NO CROSS-TALK WAS INDUCED.
THE AGING PROBLEM

1) DESCRIPTION OF THE TEST BENCH

2) RESULTS OF THE TEST BENCH

3) CONSTRAINTS FOR THE ELECTRONICS
1) DESCRIPTION OF THE TEST BENCH
2) RESULTS

- THE Ma-PMT WAS ILLUMINATED FOR ONE MONTH IN THE EXPECTED CONDITIONS (FOR THE HOTTEST CHANNEL) OF THE EXPERIMENT.

- SPECTACULAR EXPONENTIAL DROP OF THE PMT GAIN (FEW WEEKS OF LIFETIME).

- ACTIONS
  - DECREASE THE OPERATION GAIN OF THE PMT. TYPICAL GAIN IS 3000!
  - INCREASE ACCORDINGLY THE ELECTRONICS GAIN.
2) RESULTS

- NEW CAMPAIGN OF AGING TESTS WITH A GAIN DIVIDED BY TEN (ONE LHCb YEAR EQUIVALENT).
- GIVES CONFIDENCE THAT THE NEW WORKING POINT IS ADEQUATE.
- THE EFFECTS ARE UNDERSTOOD AND RELATED TO THE METAL CHANNEL DYNOodic STRUCTURE (Cs LAYER).
3) CONSTRAINTS TO THE ELECTRONICS

- The electronics was designed.

- The most elegant and rapid solution was to redesign the first stage of the Very Front End electronics.

- Keep the remaining part as it was.
NEW DESIGN OF THE ELECTRONICS

1) THE FIRST STAGE OF THE ELECTRONICS

2) THE VFE BOARD (functions and design)

3) INTEREST FOR THE LHC BEAM MONITORING

4) THE FE BOARD (functions and design)
1) FIRST STAGE OF THE VFE ELECTRONICS AND GENERALITIES

✓ FIRST STAGE INSPIRED BY THE READ-OUT CHIP OF THE TARGET TRACKER OF THE OPERA EXPERIMENT.

✓ THE CHALLENGE IS TO DEAL WITH AND MEASURE PEAK CURRENTS OF FEW HUNDREDS nA WITH AN ELECTRONICS NOISE OF 100 nA (GAIN OF THE CHIP IS 26000 OHM).

✓ THE CHIP DESIGN IS FULLY BALANCED (DIFFERENTIAL) AND DC-COUPLED FROM THE VERY BEGINNING TO THE ADC.

✓ TECHNOLOGY AMS 0.8µm BIPOLAR-CMOS.

✓ THE PMT CURRENT IS TRANSFORMED IN TWO BALANCED AMPLIFIED CURRENTS.
2) VFE BOARD: FUNCTIONNALITIES

✓ HAS TO COPE WITH SMALL AND FLUCTUATING PULSE SHAPES TOGETHER WITH LARGE SIGNAL.

✓ LARGE AND PRECISE DYNAMICS REQUIRED.

✓ MIXED ANALOG/DIGITAL SHAPING: TWO INTERLEAVED FAST INTEGRATORS @ 20 MHz, ONE BEING IN INTEGRATION MODE WHILE THE OTHER IS DIGITALLY RESET.

J. Lecoq et al. IEEE Proceedings, Colmar 2002
NEW DESIGN OF THE ELECTRONICS

2) VFE BOARD: PERFORMANCE

- INTEGRATION FOR 25 ns (ALMOST NO DEAD TIME).
- NOISE IS 1/1000 OF THE DYNAMICS.
- LINEARITY: FINE ALL ALONG THE DYNAMICS
NEW DESIGN OF THE ELECTRONICS

2) VFE BOARD: PERFORMANCE

✓ PRE-SERIES: 61 4-CHANNELS CHIPS.
✓ 2 OF 61 WERE BADLY BOUNDED.
✓ ALL OTHERS FIT NICELY THE SPECIFICATIONS.
NEW DESIGN OF THE ELECTRONICS

2) VFE BOARD: IMAGE AND PERSPECTIVES

PRODUCTION READINESS REVIEW OF THE NEW DESIGN WAS JUST HELD THE 25th OF MARCH. PRODUCTION TO BE LAUNCHED HEREAFTER.
3) VFE BOARD: APPLIED TO THE LHC MONITORING

- A 25 ns INTEGRATOR IS OF IMPORTANT INTEREST FOR LHC.
- SET A “TRANSFORMER” AROUND THE BEAM.
- LOAD A 50 Ohm RESISTOR.
- MEASURE THE NUMBER OF PROTONS IN A BUNCH. FAST LUMINOSITY MEASUREMENT.
- THE CERN ACCELERATOR TEAM ADOPTED THE FIRST VERSION CHIP OF THE PS VFE ELECTRONICS: SUCCESFULLY TESTED WITH SPS.

*R. Jones et al. IEEE Proceedings, Colmar 2002*
4) FE BOARD: FUNCTIONNALITIES (SIMPLIFIED)
PS ELECTRONICS

4) FE BOARD: PROTOTYPE USED IN Ma-PMT TB

✓ 16 channels = 4 VFE chips.

✓ Additional DAQ system
  (FPGA internal memory and VME)

✓ Was used for test beam with PS detector and VFE chip prototypes: QUALIFIED.

✓ FINAL PROTOTYPE ABOUT TO BE COMPLETED; PRR BEFORE SUMMER.
✓ PRODUCTION FORESEEN BY THE END OF THE YEAR.

R. Cornat et al. IEEE Proceedings, Colmar 2002
CONCLUSIONS

- DEDICATED PHOTODETECTOR R&D HAS BEEN CONDUCTED: 8-STAGES Ma-PMT FROM THE HAMAMATSU COMPANY FULFILL THE SPECIFICATIONS.

- WE ARE ABOUT TO ORDER THE Ma-PMT.

- PRODUCTION READINESS REVIEW OF THE NEW DESIGN OF THE VFE ELECTRONICS WAS JUST HELD THE 25th OF MARCH: PRODUCTIONS OF THE CHIPS TO BE LAUNCHED IN NEXT WEEKS.

- FINAL PROTOTYPE OF THE FE CARD ABOUT TO BE COMPLETED. PRODUCTION SHALL START THIS YEAR.

- R&D IS BASICALLY OVER. PRODUCTION TIMES…
2) VFE BOARD: PERSPECTIVES

- PRODUCTION READINESS REVIEW OF THE NEW DESIGN WAS JUST HELD THE 25th OF MARCH.

- TWO PRODUCTIONS WILL BE LAUNCHED:
  1) THE SUCCESSFULLY TESTED CHIP, FOR WHICH THE Ma-PMT NON-UNIFORMITIES ARE CORRECTED DIRECTLY ON THE VFE BOARD THANKS TO ADEQUATE RESISTORS AND CAPACITANCES.
  2) A TWO-GAINS AVATAR WHERE NON-UNIFORMITIES UP TO A FACTOR 2 ARE HANDLED WITH DEDICATED JUMPERS (BASELINE SOLUTION)
NEW DESIGN OF THE ELECTRONICS

4) FE BOARD: FUNCTIONNALITIES (greater details)
NEW DESIGN OF THE ELECTRONICS

4) FE BOARD: FUNCTIONNALITIES

✓ Mixed part
  ✓ Signal reception
  ✓ Levels adaptation
  ✓ Digitisation

✓ Digital processing
  ✓ Physics data (pedestal subtraction, spill-over correction and half channel gains adjustments)
  ✓ Trigger data: linked to SPD and ECAL
NEW DESIGN OF THE ELECTRONICS

4) FE BOARD: PERSPECTIVES

✓ FINAL PROTOTYPE ABOUT TO BE COMPLETED.
✓ PRR BEFORE SUMMER
✓ PRODUCTION FORESEEN BY THE END OF THE YEAR