The LHCb Calorimeter Triggers

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Overview of the LHCb triggers

◆ Two hardware levels

- Level 0 reduces the rate to 1 MHz in 4 μs
  - Select high $P_T$ particles
  - Reject multiple interactions

- Level 1 reduces the rate to 40 kHz in 1000 μs
  - Identification of a secondary vertex

- DAQ input at 40 kHz

◆ Software filtering

- Two software filtering stages to reduce the rate to 200 Hz
**Level 0 Trigger parameters**

- LHC repetition rate 40 MHz
  - But only ~76% have colliding bunches at LHCb

- LHCb works at 'low' luminosity, to have a single interaction per crossing
  - Nominally $2 \times 10^{32} \text{ cm}^{-2}\text{s}^{-1}$
  - Double and multiple interactions are rejected as soon as possible, using a pile-up VETO at Level 0

- Rate of interaction:
  - Single: 9.4 MHz
  - Multiple: 3.0 MHz

- Accepted rate 1 MHz
  - Factor 10 reduction on single interactions
  - In fact a bit more as multiple interactions are not all vetoed.
Level 0 Architecture

- Selection of high $P_T$ particles
  - Electrons, photons, hadrons, $\pi^0$
  - Muons
  - Total (transverse) energy may also be used.

- Detection of multiple interactions: Pile up-veto
  - Two dedicated VELO detectors upstream the interaction point
  - Histogram the Z impact of all radial hit combinations
    - Search for a second peak.
  - Rejects ~80% of the double interactions, >95% when 3 or more interactions.

- Combination and decision: the L0 Decision Unit
  - Mainly $E_T$ cuts on the various particle types
    - Adjusted during the fill to keep the output rate at 1 MHz
  - It can combine several particle types if useful.
    - It can also ignore the pile-up veto for rare cases like $B \rightarrow \mu\mu$
  - Sends decision to the Readout Supervisor
    - Accept two consecutive BX, but no more than 15 events in 900 ns due to the size of the de-randomisation buffer in the front-end cards.
Calorimeter Triggers
General principles

◆ Identify hot spots

- A shower has a 'small' size
  ¬ Detect a high energy in a small surface
  ¬ Use a square of 2 x 2 cells area
    ➤ 8 x 8 cm² in the central region of ECAL (may lose a few % of the energy)
    ➤ more than 50 x 50 cm² in the outer region of HCAL

◆ Select the particles with the highest $E_T$

- Due to its high mass, a B particle decays into high $P_T$ particles
  ¬ 'High $P_T$' is a few GeV
  ¬ For the Level 0 decision, we need only the particle with the highest $P_T$.
    ➤ Maybe also the second highest in HCAL, see later
One can then select locally the highest candidate

- Process further only these candidates
  - Reduced complexity and cabling
  - Only ~200 for ECAL and ~50 for HCAL starting from 6000 and 1500 cells.

**Validate the candidates**

- Electron, photon, $\pi^0$:
  - Electromagnetic nature using the PreShower, charge using the SPD
  - Same granularity, projective
    - Look only at the cells with the same number in the other detectors

- Hadron
  - Would like to add the energy lost in ECAL, in front of the candidate
    - Complex connectivity, expensive
  - Useful only if the ECAL contribution is important
    - If small, it can be ignored without too much harm
  - Look only at ECAL candidates!
    - Manageable number of connections
Select the highest validated candidate

- One wants simple decisions at this early level
- Using the second highest hadron was shown to improve marginally the efficiency in some cases.
  - The studied implementation allows to produce this second highest.
  - No need for a second highest electron or photon.
- The number of links, and consequently the cost is by far smaller if one reduces locally the number of candidates…

Processing entirely synchronous

- No dependence on occupancy and on history
  - Easier to understand and to debug
- Pipeline processing at all stages.
Inputs

- About 6000 ECAL cells (same number for PreShower and SPD)

- Front-end electronics located on top of the detector
  - Order of 100 rads / 10 years

- We want to minimise cabling complexity
  - Integrate the first selection in the front-end card.

- Quantity to manipulate: $E_T$, converted from the ADC by a dedicated LUT.
  - 8 bits are OK, with full scale around 5 GeV.

- Use a dedicated backplane for as many connections as possible
  - Use LVDS levels, multiplexed signals, as soon as there are several bits
Synopsis of LHCb ECAL & HCAL Front-end Board

Front Panel Connector (32 channels from PMs)
Shaper
ADC 12bits/40Mhz
convert
Pedestal subtraction
PGA
RAM 32K/8b
12
13
SPL
32
Odd pulser
Even pulser
Fonctionnal internal calibration mode
External trigger
External Clock
Internal trigger
Test
JTAG bus
Command
Local data bus
40Mhz_clock
FPGA 3256-100/Eeprom
Serial interface
Decoder
GTL+ to Validation card
Fifo
32k/14b
384Db
128/12
16
Card controller PGA Flex
L0 Latency
1024/12
L0 Derandomiser buffer
16/12
40 Mhz_clock
Control signals
Bc id & Evt id
(4*8):9Dp LVDS+9*8DbGTL+

Serial Data Bus
L1 seq
L1 latency
PL
Point to point LVDS links
To L1 buffer
Flex 6016/240
8sums/Comp
Flex 6016/240
8sums/Comp
Flex 6016/240
8sums/Comp
Fifo
32k/16
SPL

Monitoring Fifo
BC & Evt id

GTL+ to Validation card
LVDS to Hcal
LVDS to PS

Functinal internal calibration mode
Intrinsic trigger
External trigger
Test

GTL+ to Validation card
Trigger Test mode
Subtraction Enable
L1 Demorandomiser
buffer
L0 Latency pipeline
129/12
Flex 6016/240
8sums/Comp
40 Mhz_clock
Crate Controler Link
(4*8):9Dp LVDS+9*8DbGTL+

Flex 6016/240
8sums/Comp
Flex 6016/240
8sums/Comp
Flex 6016/240
8sums/Comp

SPL

SPL

SPL

SPL
**First selection**

**Build the 2x2 sums**

- Work inside a 32 channels (8x4) front-end card
  - To obtain the 32 2x2 sums, one needs to get the 8 + 1 + 4 neighbours
  - Via the backplane (9) or dedicated point-to-point cables (4)

![Diagram of 2x2 sums and neighbours]

- Neighbours of each cell
- 8 bits LVDS multiplexed link
- 8 bits on the backplane
Select the local maximum in the card

- Simple comparison of the summed $E_T$.
- Currently implemented in 4 ALTERA FPGA’s, could be simplified when bigger FPGA’s are available.

The 32 $2^2$ sums are compared and the highest one selected by 4 FPGAs. This is performed in 10 clock cycles, without taking into account the time, to get the neighbour information.
ECAL validation

For each candidate, one needs to access the PSD+PreShower information, i.e. 2 times 4 bits.

The address of the candidate is sent from the ECAL to the PreShower FE card

- One PreShower card handles 64 channels, exactly 2 ECAL cards.

The 2x4 bits are extracted synchronously at each BX and sent to the Validation Card
A decision is then taken to validate the ECAL candidate as photon, electron or nothing.

- PreShower + SPD => electron
- PreShower alone => photon
- Possible VETO on dirty cases, to reject splashes
- Validation by a LUT (8 bits input, 2 outputs) => flexibility

Only the highest electron and the highest photon are kept.

\[ \pi^0 \text{ trigger} \]

- Combine two photons from neighbouring ECAL cards
- Not very efficient, but selects easy-to-reconstruct \( \pi^0 \)s
- This idea is still under study.
**HCAL validation**

- One wants to add the ECAL candidate in front of the HCAL one

- It was found easier to bring the HCAL candidates to a place where the ECAL candidates are available! Even if some have to be duplicated
  - About 200 ECAL candidates
  - About 50 HCAL candidates
  - Including the needed duplication, one has 80 links HCAL to ECAL, instead of 200 links ECAL to HCAL

- The ECAL and HCAL addresses are matched (LUT) and the $E_T$ of the highest matching ECAL candidate is added to the HCAL one.

- All candidates are sent to the barracks, for later processing.
Select the final candidates

- Easy for electron, photon, $\pi^0$: Only the one with highest $E_T$ is kept.
- For HCAL: The highest is also easy.
- The second highest implies to remove ‘ghosts’
  - 1- The same HCAL candidate may go to two Validation Cards.
  - 2- The same cell can be used by two candidates in neighbouring FE cards
Removing ghosts is just checking if the addresses differs by no more than ±1 in row and column.

We want the total $E_T$ and the seeds for 'super-L1', where the first type of ghosts (from the same HCAL card) have to be always removed.

* We know where are the two candidates coming from the same HCAL card.
  - Just select the one with highest $E_T$. 
Performances

 puedty is OK

- The number of clock cycles needed is sensibly below the allowed budget.

Compare to minimum bias retention

- The constraint is to keep the Level 0 rate to 1 MHz
  - This defines the rejection factor on minimum bias
  - The sharing between the various types of particles is being optimised.
    - The rejection should be about 15 for hadron, 100 for electron and 200 for photon / $\pi^0$
- The plots show the minimum bias rejection and the signal acceptance versus the $E_T$ cut.
  - 'Signal' is normalised to events which can be reconstructed in LHCb
- This is only the Level 0 acceptance.
From right to left on the figure:
- For a given rejection, read the $E_T$ threshold
- For this threshold, read the signal efficiency

$B_d \rightarrow \pi\pi$

$B_d \rightarrow J/\Psi(e^+e^-) K^0_S$
Conclusions

We have a powerful Calorimeter Trigger

- It minimises the number of connections.
  * Less that 1000 LVDS links between cards on the same Calorimeter platform
  * About 150 optical links to the barracks.

- Many connections on the backplane
  * Same crates for ECAL, HCAL and PreShower electronics.

- It could be built almost now
  * But no need to hurry, we need it in 2004 only
  * New FPGA’s may simplify the design, and gain some speed, even if this doesn’t seem to be needed

- It performs very well.