LHCb and its electronics

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On behalf of the LHCb collaboration
Physics background

- CP violation necessary to explain matter dominance
- B hadron decays good candidate to study CP violation
- B lifetime ~1ps -> short decay length (few mm)
- 40 - 400 tracks per event
LHCb differences from ATLAS/CMS

- ~1/4 size: budget, physical size, number of collaborators
- 1.2 million channels in 9 different sub-detectors
- Particle identification vital -> RICH detectors
- Vertex resolution vital -> Vertex detector in secondary machine vacuum
- Uses existing DELPHI cavern: reduced cost, must adapt
- Open detector with “fixed target topology” (easy access, sub-detectors mechanically “independent”, flexible assembly)
- Forward angle detector -> high particle density
- B physics triggering difficult -> 4 trigger levels with two in front-end
- One interaction per ~3 bunch crossings to prevent overlapping events in same crossing (ATLAS/CMS: factor ~50 higher)
- First level (L0) trigger rate of 1 MHz (ATLAS/CMS: factor 10 - 20 lower)
- Consecutive first level triggers supported (ATLAS/CMS: gap of 3 or more)
- First and second level trigger (L0 & L1) buffering in front-end
LHCb evolution since LEB 97

- September 1998 LHCb approved
- General architecture maintained
- Most detector technologies now defined
- Key front-end parameters defined
- L0 latency 3 µs -> 4 µs
- L1 latency 50 µs -> 1000 µs (memory cheap)
- Buffer overflow prevention schemes defined:
  - Front-end control defined (TTC, partitioning, overflow prevention, etc.)
- Electronics under development
- Better understanding of radiation environment (but more work needed)
- L2 and L3 trigger performed on same physical processor
- Architecture of trigger implementations defined
- Push architecture for DAQ event building network maintained
- Standard interface and data merger module to DAQ under design
- Start to make TDR’s.
LHCb detector in DELPHI cavern

LHC-B Detector

Detector characteristics
- Width: 18m
- Length: 12m
- Height: 12m
- Weight: 4270t
Front-end and DAQ architecture

- 1.2 million channels
- 4 µs analog or digital
- 16 events
- 40 K “links” analog/digital
- 1000 events (digital)
- ~10 events Few hundred links

Clock pipelined processing and buffering

Front-end simulated in VHDL
L1 trigger simulated in Ptolemy

Parallel processing in L1 trigger system
Event “pipelined” buffering in front-end

Front-end 
DAQ
Parallel processing

Event building network: 4GB/s
Event buffers
L2 & L3
CPU X 1000
200Hz x 100KB
Front-end buffer control

L0 pipeline

L0 trigger

Readout supervisor

Veto's all L0 trigger accepts that risk to overflow L0 derandomizers

All L0 derandomizers must comply to given rule:
Minimum depth: 16 events
Maximum readout time: 900ns = (32+4)x25ns

L0 Derandomizer loss vs Read out speed

Depth = 4
Depth = 8
Depth = 16
Depth = 32

Data merging

32 data 4 data tags (Bunch ID, Event ID, etc.)

Data @ 40MHz

Derand.

1MHz

32

Not full

X 32

Same state
Consecutive L0 triggers

- Gaps between L0 triggers would imply ~3% physics loss per gap at 1MHz trigger rate.
- Problematic for detectors that need multiple samples per trigger or detectors with drift time.
  - All sub-detectors have agreed that this can be handled
- Very useful for testing, verification, calibration and timing alignment of detectors and their electronics

Max 16 consecutive triggers

![Graph showing time alignment, pulse width, and baseline shifts.](image)
L1 buffer control

4 tags
32 data
L1 buffer

Max
1000 events

900ns per event
36 words per event @ 40MHz

L1 trigger

Vertex

Event N
CPU

Event N+1
CPU

Reorganize

L1 buffer monitor
(max 1000 events)

L1 decision
spacing (900ns)

L1 Throttle
accept -> reject

Throttle
L0 triggers

40 kHz

Nearly full

Board

System

History trace

TTC broadcast (400ns)

Nearly full

DAQ

Data merge

Output buffer

Zero-suppression
< 25 µs

L1 derandomizer

Data to DAQ

LEB 2000 Cracow

J. Christiansen
Readout supervisor

- Main controller of front-end and input to DAQ
- Receive L0 and L1 trigger decisions from trigger systems.
- Restrict triggers to prevent buffer overflows in front-end, L1 trigger and DAQ
  - L0: Derandomizer emulation + Throttle
  - L1: Throttle
- Generate special triggers: calibration, empty bunch, no bias, etc.
- Reset front-end
- Drive TTC system via switch.
- Allow flexible partitioning and debugging
  - One readout supervisor per partition
  - Partitioning of throttle network
  - Partitioning of TTC system
DAQ

~1000 front-end sources

Front-end multiplexing based on Readout Unit

~100 readout units

4GB/s

~100 CPU farms

~1000 CPU's of 1000MIPS or more

Event building network (100 x 100)

Front-end multiplexing based on Readout Unit

< 50MB/s per link

~100 CPU farms

~1000 CPU's of 1000MIPS or more
Experiment control system (ECS)

ECS controls and monitors everything in LHCb
  - DAQ (partitioning, initializing, start, stop, running, monitoring, etc.)
  - Front-end and trigger systems (initializing, calibration, monitoring, etc.)
  - Traditional slow control (magnet, gas systems, crates, power supplies, etc.)

Requirements
  - Based on commercial control software (from JCOP)
  - Gbytes of data to download to front-end, trigger, DAQ, etc.
  - Distributed system with ~one hundred computers/processors.
  - Partitioning into “independent” sub-systems (commissioning, debugging, running)
  - Support standard links (Ethernet, CAN, etc.)
ECS interface to electronics

- No radiation (counting room):
  Ethernet to credit card PC on modules
  Local bus: Parallel bus, I²C, JTAG

- Low level radiation (cavern):
  10Mbits/s custom serial LVDS twisted pair
  SEU immune antifuse based FPGA interface chip
  Local bus: Parallel bus, I²C, JTAG

- High level radiation (inside detectors):
  CCU control system made for CMS tracker
  Radiation hard, SEU immune, bypass
  Local bus: Parallel bus, I²C, JTAG

Support

- Supply of interface devices (masters and slaves)
- Software drivers, software support
Radiation environment

In detector: 1K - 1M rad/year
  - Analog front-ends
  - L0 pipeline (Vertex, Inner tracker, RICH)

Repair: Few days to open detector

Edge of detector and in nearby cavern:
Few hundred rad/year
\(\sim 10^{10} \text{ 1Mev neutrons/cm}^2\text{year}\)
  - L0 pipelines
  - L0 trigger systems
  - L1 electronics
  - Power supplies ? (reliability)

Access: 1 hour with 24 hour notice
  Quick repairs must be possible
  Remote diagnostics required

SEU problems:
  - Control flip-flops
  - Memories
  - FPGA's

MARS '97(HEP): LHC-B absorbed dose levels map
Electronics in cavern

- Relatively low total dose
- Relatively low neutron flux
- Complex L0 trigger system and L0 and L1 electronics in cavern
  -> SEU becomes problematic

Use of COTS justified

Hadron flux at edge of calorimeter: $\sim 3 \times 10^{10}$ part./cm$^2$/year, $E > 10$ Mev

Upset rate:
  Module: $3 \times 10^{10} \times 4 \times 10^{-15} \times 10^7 = 1200$ per year (once per few hours)
  System: $1200 \times 1000 = 1.2$ million per year (few per minute)

Recovery only by re-initialization !!.

Assumptions: Data memory not considered
  32 FPGAs used for control & ZS
  300 Kbit programming per FPGA
  Total 10Mbits per board
  1000 modules in total system

Typical L1 front-end board

Xilinx

Xlinx

~1000 channels

L1 buffer

Zero suppression

control

X 32

~32

~1000 channels
Errors

• Monitoring
  – Assume soft errors from SEU and glitches
  – All event fragments must contain Bunch ID, Event ID plus option of two more tags (error flags, check sum, buffer address, etc).
  – Errors in data “ignored”
  – Errors in control fatal:
    • All buffer overflows must be detected and signaled (even though system made to prevent this)
    • When merging data, event fragments must be verified to be consistent
    • Self checking state machines encouraged (one hot encoding)
    • Continuous parity check on setup parameters encouraged

• Recovery
  – Quick reset of L0 and L1 front-ends specified
  – Fast download of front-end parameters
  – Local recovery considered dangerous
In-situ testing

- All registers must have read back
- Never mix event data and system control data
- Effective remote diagnosis for electronics in cavern to enable quick repairs (1 hour)
  - Sub-systems
  - Boards
  - Data links
  - Power supplies
- Use of JTAG boundary scan encouraged (also in-situ)
ASIC’s

• Needed for required performance
• Needed for acceptable cost (but ASIC’s are expensive)
• Problematic for time schedules
  – 1 year delay in designs can easily accumulate.
  – Time for testing and qualification often underestimated.
  – Remaining electronics can not advance before ASIC’s ready.
  – Design errors can not be corrected by “straps”.
  – Technologies are quickly phased out in today’s market (5 years).
  – Use of single supplier potentially dangerous.

• All sub-detectors rely on one or a few key ASIC’s

• ASIC’s in LHCb:
  – Designs: ~10
  – Total volume: ~ 50 K
  – Technologies: 4 x 0.25 μm CMOS, DMILL, BiCMOS, etc.
  – Prototypes of most ASIC’s exist

We are a very small and difficult customer that easily risks to be put at the bottom of the manufactures priority list
Where are we now

• Progressing towards TDR’s over coming year.
  Long production time -> now
  Short production time -> later

• Architecture and parameters of Front-end, trigger and DAQ systems defined.

• Working on prototypes of detectors and electronics.

• Ready to select ECS system
  Part of JCOP
  Standardizing ECS interfaces to front-ends.

• Event building network of DAQ not yet chosen
  Uses commercial technology which must be chosen at the latest possible moment to get highest possible performance at lowest prices
  (Gigabit Ethernet or alike)
A few implementations

- Beetle silicon strip front-end in 0.25 µm CMOS
- Vertex detector prototype with SCTA front-end
- Vertex vacuum tank

Used in 2 (3) LHCb detectors
Backup in DMILL (SCTA-VELO)
RICH detector

Pixel chip in 0.25 um CMOS is a common development with ALICE

Critical time schedule as integrated into vacuum tube

Backup solution using commercial MAPMT, read out by analog pipeline chip (Beetle or SCTA-VELO)
Hcal & Ecal 40 MHz 12bits front-end

Readout Unit: data concentration & DAQ interface
## LHCb electronics in numbers

<table>
<thead>
<tr>
<th>Category</th>
<th>Quantity/Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channels</td>
<td>1.2 million</td>
</tr>
<tr>
<td>Sub-detectors</td>
<td>9</td>
</tr>
<tr>
<td>Triggers</td>
<td>4</td>
</tr>
<tr>
<td>Rates</td>
<td>1 MHz, 40 kHz, 5 kHz, 200 Hz</td>
</tr>
<tr>
<td>Latencies</td>
<td>4 µs, 1 ms, 10 ms, 200 ms</td>
</tr>
<tr>
<td>Event size</td>
<td>100 Kbyte</td>
</tr>
<tr>
<td>ASIC’s</td>
<td>50K in 10 different types</td>
</tr>
<tr>
<td>TTCrx</td>
<td>2000</td>
</tr>
<tr>
<td>Data links</td>
<td>2000 optical + 40K short distance analog or LVDS</td>
</tr>
<tr>
<td>9U modules</td>
<td>1000 FE + 100 L0 + 100 RU + 50 control</td>
</tr>
<tr>
<td>Racks</td>
<td>30 cavern, 80 underground counting room, 50 surface (DAQ)</td>
</tr>
<tr>
<td>CPU’s</td>
<td>100 L1 + 1000 DAQ + 100 ECS + FE DSP</td>
</tr>
</tbody>
</table>
# Electronics status

<table>
<thead>
<tr>
<th>System</th>
<th>FE architecture</th>
<th>Status</th>
<th>TDR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Front-end</td>
<td>Common definitions</td>
<td>Architecture and parameters defined</td>
<td></td>
</tr>
<tr>
<td>L0 trigger</td>
<td>Pipelined</td>
<td>Architecture defined, Simulations</td>
<td>Early 02</td>
</tr>
<tr>
<td>L1 trigger</td>
<td>Parallel CPU's</td>
<td>Architecture defined, Simulations + prototyping</td>
<td></td>
</tr>
<tr>
<td>DAQ</td>
<td>Parallel, data push</td>
<td>Architecture defined, Simulations</td>
<td>Early 02</td>
</tr>
<tr>
<td>Vertex</td>
<td>Analog readout</td>
<td>FE chip prototypes under test</td>
<td>Mid 01</td>
</tr>
<tr>
<td>RICH</td>
<td>Binary pixel + backup</td>
<td>FE chip prototype to be tested</td>
<td>Sep 00</td>
</tr>
<tr>
<td>Inner tracker</td>
<td>Same as Vertex</td>
<td>Defining detector type (substitute for MSGC)</td>
<td>End 01</td>
</tr>
<tr>
<td>Outer tracker</td>
<td>ASD + TDC</td>
<td>Selecting ASD, TDC chip to be tested</td>
<td>Mid 01</td>
</tr>
<tr>
<td>Preshower + E/H cal</td>
<td>Digital 10 bit</td>
<td>FE prototypes tested</td>
<td>Sep 00</td>
</tr>
<tr>
<td></td>
<td>Digital 12 bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Muon</td>
<td>Binary</td>
<td>Architecture + FE under study</td>
<td>Early 01</td>
</tr>
</tbody>
</table>
Worries in LHCb electronics

- Time schedules of ASIC’s may easily become critical
- Correctly quantify SEU problem in LHCb cavern
- Use of power supplies in LHCb cavern
- Support for common projects:
  TTC, radiation hard 0.25 um CMOS, power supplies, ECS framework
- Limited number of electronics designers available
  - Limited electronics support available from CERN
  - Limited number of electronics designers in HEP institutes
  - Difficult to involve engineering institutes/groups
    - No funding for HEP electronics
    - Prefer to work on industrial problems
    - Prefer to work on specific challenges in electronics
    - Hard to get electronics designers and computer scientists (booming market)
- Qualification/verification of ~10 ASIC designs, tens of hybrids and tens of complicated modules.
- Documentation and maintenance
- Supply of electronics components expected to become very difficult for small consumers in the coming two years
Handling electronics in LHCb

- Electronics community in LHCb sufficiently small that general problems can be discussed openly and decisions can be reached.
- Regular electronics workshop of one week dealing with front-end, trigger, DAQ and ECS.
- Specific electronics meeting (1/2 day) during LHCb weeks with no parallel sessions to allow front-end, trigger, DAQ, ECS to discuss electronics issues.
- Electronics coordination part of technical board.
- It is recognized that electronics is a critical (and complicated and expensive and ----) part of the experiment.
- Review policy agreed upon (but not yet used extensively)
  Architecture, Key components (ASIC’s, boards), Production readiness